CLAIMS

What is claimed is:

1. A memory controller system, comprising:

a plurality of memory controller subsystems coupled to a plurality of computer components, each memory controller subsystem including:

at least one read or write queue with an input coupled to one of the computer components and an output coupled to memory for queuing read or write commands to be sent to the memory, and

at least one activate queue with an input coupled to one of the computer components and an output coupled to the memory for queuing activate commands to be sent to the memory;

wherein the activate commands are capable of being restored to a row and a bank associated with the read or write commands at a head of the associated read or write queue.

2. The memory controller system as recited in claim 1, wherein the computer components are selected from the group consisting of a central processing unit, a display refresh module, and a graphics unit.

3. The memory controller system as recited in claim 1, wherein the memory includes dynamic random access memory (DRAM).

4. The memory controller system as recited in claim 1, wherein the memory includes synchronous dynamic random access memory (SDRAM).

5. The memory controller system as recited in claim 1, wherein each memory controller subsystem further includes a multiplexer having inputs coupled to the outputs of the

read or write queue, and activate queue, the multiplexer further including an output coupled to the memory.

6. The memory controller system as recited in claim 1, wherein the read or write commands, and the activate commands of each memory controller subsystem are loaded independent of the state of the memory.

7. The memory controller system as recited in claim 1, wherein the commands are loaded in at least one of the queues of each memory controller subsystem based on rows and banks of references in at least one of the queues.

8. The memory controller system as recited in claim 1, wherein the loading of the commands in at least one of the queues of each memory controller subsystem is delayed based on rows and banks of references in at least one of the queues.

9. The memory controller system as recited in claim 1, wherein each read or write queue is permitted to queue commands for only a single row in each bank.

10. The memory controller system as recited in claim 1, wherein the computer components include a central processing unit, a display refresh module, and a graphics unit.

11. The memory controller system as recited in claim 1, wherein the memory controller system arbitrarily selects to unload commands from queues associated with any of the computer components.

12. A method for controlling memory utilizing a memory controller, comprising:

receiving a plurality of read or write commands, and activate commands from a plurality of queues capable of being loaded from a plurality of computer components;

arbitrating the delivery of the read or write commands, and activate commands from the queues to the memory; and

delivering the arbitrated read or write commands, and activate commands to the memory;

wherein the memory controller is capable of restoring the activate commands to a row and a bank associated with the read or write commands at a head of a read or write queue.

13. The method as recited in claim 12, wherein the computer components are selected from the group consisting of a central processing unit, a display refresh module, and a graphics unit.

14. The method as recited in claim 12, wherein the memory includes dual data rate (DDR) memory.

15. The method as recited in claim 12, wherein the memory includes dynamic random access memory (DRAM).

16. The method as recited in claim 12, wherein the memory includes synchronous dynamic random access memory (SDRAM).

17. The method as recited in claim 12, wherein the delivery of the read or write commands, and activate commands from the queues to the memory is arbitrated utilizing a timer.

18. The method as recited in claim 17, wherein the timer arbitrates the delivery of the commands to ensure that sequential commands are delivered sequentially.

19. The method as recited in claim 12, wherein the delivery of the read or write commands, and activate commands from the queues to the memory is arbitrated based on a predetermined order.

20. The method as recited in claim 12, wherein the delivery of at least one of the commands is arbitrated based on a bank and a row at a head of the queues.

21. The method as recited in claim 12, wherein the delivery of at least one of the commands is arbitrated based on the read or write commands.

22. The method as recited in claim 19, wherein the predetermined order prioritizes the computer components.

23. The method as recited in claim 19, wherein the predetermined order prioritizes the read or write commands, the activate commands.

24. A method, comprising:

providing at least three parallel-coupled memory controller subsystems each capable of:

queuing read or write commands to be sent to the memory in at least one read or write queue with an input coupled to a computer component and an output coupled to memory, and

queuing activate commands to be sent to the memory in an activate queue with an input coupled to the computer component and an output coupled to the memory,

wherein a first one of the memory controller subsystems is coupled to a graphics unit computer component, a second one of the memory controller subsystems is coupled to a central processing computer component, and a third one of the memory controller subsystems is coupled to a display refresh module computer component.

25. A memory controller system, comprising:

at least three memory controller subsystems coupled to a plurality of computer components;

wherein a first one of the memory controller subsystems is coupled to a graphics unit computer component, a second one of the memory controller subsystems is coupled to a central processing computer component, and a third one of the memory controller subsystems is coupled to a display refresh module computer component.